Patents

Patents **111** - **120** on **TRANSMITTER AND RECEIVER: ACK AND NACK**. (**0.05** seconds)

Did you mean: ***TRANSMITTER AND RECEIVE: ACK AND NECK***

Transmitter, **receiver**, and coding scheme to increase data rate and decrease bit error rate of an ...
US Pat. 6851086 - Filed Mar 30, 2001
If an **ACK** is received the appropriate packet manager 262 is signaled to clear its buffer and enter the idle state. If an **NACK** is received, the appropriate ...

Random access control method for CDMA system
US Pat. 7133387 - Filed Apr 11, 2001 - NEC Corporation
Transmitter/receiver of base station 1 in the base station 45 is provided ...
Code generation unit 15 generates **ACK** signal or **NACK** signal on the basis of ...

Formation of rekey messages in a communication system
US Pat. 5164986 - Filed Feb 27, 1991 - Motorola, Inc.
A **transmitter** 217 and **receiver** 219 modulate and demodulate data, respec- 30 lively, ... The KMC then checks for reception of an **ACK** or **NACK** at step 419. ...

Method and system for a data transmission in a communication system
US Pat. 7050405 - Filed Dec 6, 2002 - Qualcomm Incorporated
The reverse link packet error rate is determined in accordance with **ACK/NACK** of the reverse link packets. The value of A is increased by a first determined ...

Method and protocol to support contention-free intervals and QoS in a CSMA network
US Pat. 6907044 - Filed Aug 4, 2000 - Intellon Corporation
The "partial ARQ" allows a **transmitter** to known that at least one station ...
101 Frame response with **ACK/NACK**/FAIL (same as above) to be followed by ...

Assuring sequence number availability in an adaptive hybrid-ARQ coding system
US Pat. 6519731 - Filed Oct 22, 1999 - Ericsson Inc.
If there is packet data residing within the retransmission buffer 120, control transfers to box 320 in which a determination is made whether an **ACK** or **NACK** ...

Method and apparatus for time-based reception of transmissions in a wireless communication system
US Pat. 6839566 - Filed Aug 16, 2001 - QUALCOMM, Incorporated
At time t!4 the **receiver** receives the retransmitted segment, and sends an **ACK** at time t!5. The **transmitter** receives the **ACK** from time t!7 to 60 t!8. ...

Method or communications system using a robust diversity combination
US Pat. 7136424 - Filed Jun 29, 2001 - Siemens Aktiengesellschaft
To identify the packet data units arriving at the **receiver**, the units are ...
(**ACK/ NACK**) by the receiving station MS from the transmitting station BS. ...

Advanced data link controller having a plurality of multi-bit status registers
US Pat. 4368512 - Filed Mar 21, 1980 - Motorola, Inc.
The **receiver**, having acquired the block, checks for errors and then sends an **ACK** control character to the **transmitter** indicating that the block is correct ...

Method for eliminating a receiving data unit as a source of excessive resend requests
US Pat. 5636230 - Filed Jun 11, 1996 - Motorola, Inc.
-j^ preset invention can be more fully described with Upon reception of a **NACK**, the **transmitter** may resend the reference to FIGS. 1-. FIG. ...

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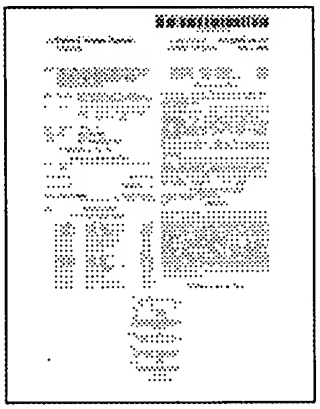
Transmitter, receiver, and coding scheme to increase data rate and decrease bit error rate of an ...

Ted Szymanski

Patent summary



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Abstract | Drawing | Description | Claims

Abstract

Transmitters, receivers, and coding schemes to increase data rate and decrease bit error rate of an optical data link are disclosed. Data is transmitted across the link with a less than nominal bit error rate (BER), by encoding the data using a forward error correction (FEC) code or by requesting retransmission of transmitted packets in error. Data is transmitted at a speed that introduces errors at a rate that is in excess of the nominal BER but that may be corrected using the FEC code or retransmission so that the data may be received with less than the nominal BER. The data rate is increased as the link operating speed is increased beyond the overhead required by the FEC codes or retransmission. High speed FEC encoders and decoders facilitating such transmission are disclosed.

Patent number: 6851086
Filing date: Mar 30, 2001
Issue date: Feb 1, 2005

Claims

What is claimed is:

1. A high-speed pipelined forward error correcting (FEC) encoder, for encoding k bit blocks of data into n bit blocks, each of said n bit blocks comprising one of said k bit blocks of data and (n−k) parity bits, said encoder comprising

Q latches, wherein Q≧3;

Q−1 combinational logic circuits, each of said combinational logic circuits interconnected between two of said latches, to receive an input of at least k bits from an upstream one of said latches, and provide an output of n bits to a downstream one of said latches, each output comprising (n−k) output bits representing said (n−k) parity bits in various stages of computation, each of said combinational logic circuits arranged to compute said (n−k) output bits in accordance with a defined generator polynomial, with said defined generator polynomial being identical for each of said combinational logic circuits.

2. The encoder of claim 1, wherein said defined generator polynomial is a generator polynomial for a cyclic code.

3. The encoder of claim 2, wherein said defined generator polynomial is a generator polynomial for a Reed-Solomon code.

4. The encoder of claim 1, wherein said defined generator polynomial generates one of a cyclic BCH code, or a cyclic Hamming code.

5. The encoder of claim 4, wherein said defined generator polynomial is a generator polynomial for one of a (7,4) Hamming code, a (15,11) Hamming code, a (15,7,2) Hamming code, a (15,7,2) BCH code, a (15,5,3) BCH code, a (31,16) BCH code, a (31,11) BCH code, a (23,12) Golay code.

6. The encoder of claim 1, wherein said FEC code is one of a (15,7), (15,5), (31,16), (63,48), (63,51), (63,45), (63,42), (63,37), (63,13), (127,113), (127,99), (127,106), and (127,64) majority-logic decodable cyclic FEC code.

7. A method of encoding k bit blocks of data into n bit blocks, each of said n bit blocks comprising one of said k bit blocks of data and (n−k) parity bits, said

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Primary Examiner: David Ton

Current U.S. Classification
714/781; 714/786

International Classification
H03M 1300

Search within this patent

Search

Citations

Patent Number	Title	Issue date
4486739	Byte oriented DC balanced (0,4) 8B/10B partitioned block transmission code	Dec 4, 1984
4777635	Reed-Solomon code encoder and syndrome generator circuit	Oct 11, 1988
5068854	Error detection for fiber distributed interfaced optic link	Nov 26, 1991
5383204	Parallel encoding apparatus and method implementing cyclic redundancy check and Reed-Solomon codes	Jan 17, 1995
5432630	Optical bus with optical transceiver modules and method of manufacture	Jul 11, 1995
5524218	Dedicated point to point fiber	Jun 4, 1996

	optic interface	
5579426	Fiber image guide based bit-parallel computer interconnect	Nov 26, 1996
5581566	High-performance parallel interface to synchronous optical network gateway	Dec 3, 1996
5606725	Broadband network having an upstream power transmission level that is dynamically adjusted as a function of the bit error rate	Feb 25, 1997
5754563	Byte-parallel system for implementing reed-solomon error-correcting codes	May 19, 1998
5943361	System and method for generating signal waveforms in a CDMA cellular telephone system	Aug 24, 1999
6031644	Method, device, and system for controlling wavelength of optical signal	Feb 29, 2000
6058499	Error correcting method and device	May 2, 2000
6070074	Method for enhancing the performance of a regenerative satellite communications system	May 30, 2000
6148423	Signal transmission performance	Nov 14, 2000

	optimization device in a system for transmitting digital data, especially on an optical link	
6438723	Method and arrangement for the reliable transmission of packet data	Aug 20, 2002
6507927	Method and device for estimating the reliability of a decoded symbol sequence	Jan 14, 2003
6683855	Forward error correction for high speed optical transmission systems	Jan 27, 2004

Referenced by

Patent Number	Title	Issue date
6956642	Error function analysis of optical components	Oct 18, 2005
7007223	Efficient method and apparatus for low latency forward error correction	Feb 28, 2006
7020567	System and method of measuring a signal propagation delay	Mar 28, 2006
7187435	Error function analysis of optical components	Mar 6, 2007

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6974928	ack or acknowledge or nack or no ackknowledge	US-PGPUB; USPAT; USOCR	OR	OFF	2007/07/16 10:10
S2	3101710	S1 and transmit$3 near multipl$3 or pluralit$3 adj packet or block or data	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 10:12
S3	1100390	S2 and multiple or plural near3 path	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 10:16
S4	207587	S3 and receiver	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 10:40
S5	56537	S4 and network	USPAT	OR	OFF	2007/07/16 10:58
S6	43	S5 and repeater adj transceiver	USPAT	OR	OFF	2007/07/16 11:05
S7	6974928	ack or acknowledge or nack or no ackknowledge	US-PGPUB; USPAT; USOCR	OR	OFF	2007/07/16 11:03
S8	3101710	S7 and transmit$3 near multipl$3 or pluralit$3 adj packet or block or data	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 11:03
S9	1100390	S8 and multiple or plural near3 path	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 11:06
S10	207587	S9 and receiver	US-PGPUB; USPAT; USOCR	OR	ON	2007/07/16 11:06
S11	56537	S10 and network	USPAT	OR	OFF	2007/07/16 11:06
S12	43	S11 and repeater adj transceiver	USPAT	OR	OFF	2007/07/16 11:06
S13	43	S11 and repeater adj transceiver	USPAT	OR	OFF	2007/07/16 11:09